



## A circular stamp from the Office of Intellectual Property (OIP). The text "OIP" is at the top, "JUL 01 2005" is in the center, and "OFFICE OF INTELLECTUAL PROPERTY" is around the bottom edge.

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Printed Name \_\_\_\_\_

6/28/2005  
Date

**Title: CIRCUITRY AND METHOD  
TO PROVIDE A HIGH  
SPEED COMPARATOR FOR  
AN INPUT STAGE  
OF A LOW-VOLTAGE  
DIFFERENTIAL SIGNAL  
RECEIVER CIRCUIT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Please find attached a Power of Attorney with regard to the above-identified patent application. Applicant respectfully requests the Commissioner to change the correspondence address for the above identified patent application. The old correspondence address was:

SIERRA PATENT GROUP, LTD.  
P O BOX 6149  
STATELINE NV 89449

The new correspondence address is:

B. Noël Kivlin  
Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.  
P.O. Box 398  
Austin, Texas 78767-0398  
(512) 853-8840

If there are any questions regarding this matter, please contact me at the telephone number provided below.

Respectfully submitted,



Jeffrey C. Hood  
Registration No. 35,198  
ATTORNEY FOR APPLICANTS

Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.  
P.O. Box 398  
Austin, TX 78767-0398  
(512) 853-8800  
Date: 6/29/2005



PATENT  
5957-16000

**POWER OF ATTORNEY; NOTICE OF CHANGE OF ADDRESS**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**POWER OF ATTORNEY**

STELLAR KINETICS LLC hereby revokes any previous Powers of Attorney and appoints the following attorneys and/or agents in connection with any and all patent applications and patents, owned by STELLAR KINETICS LLC, that are filed with the United States Patent and Trademark Office: (1) the practitioners at Customer Number 35690; and (2)

|                     |                 |
|---------------------|-----------------|
| Mark K. Brightwell  | Reg. No. 47,446 |
| Kay A. Colapret     | Reg. No. 52,759 |
| Steve J. Curran     | Reg. No. 50,664 |
| Mark R. DeLuca      | Reg. No. 44,649 |
| Heather L. Flanagan | Reg. No. 54,101 |
| Russell Henrichs    | Reg. No. 50,354 |
| Erik A. Heter       | Reg. No. 50,652 |
| Jeffrey C. Hood     | Reg. No. 35,198 |
| Rajiv Jauhari       | Reg. No. 55,850 |
| B. Noël Kivlin      | Reg. No. 33,929 |
| Robert C. Kowert    | Reg. No. 39,255 |
| Mario J. Lewin      | Reg. No. 54,268 |
| Lawrence J. Merkel  | Reg. No. 41,191 |
| Eric B. Meyertons   | Reg. No. 34,876 |
| Neal E. Persky      | Reg. No. 53,452 |
| Liza Philip         | Reg. No. 51,352 |
| David W. Quimby     | Reg. No. 39,338 |
| Rory D. Rankin      | Reg. No. 47,884 |
| Gareth Sampson      | Reg. No. 52,191 |
| Chris Thompson      | Reg. No. 43,188 |
| Mark S. Williams    | Reg. No. 50,658 |

each an attorney or agent of the firm of MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C., as its attorney or agent for so long as they remain with such firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Please direct all communications as follows:

**Customer No. 35690**

B. Noël Kivlin, Esq.

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.

P.O. BOX 398

AUSTIN, TEXAS 78767-0398

(512) 853-8840 (voice)

(512) 853-8801 (facsimile)

**CHANGE OF ADDRESS**

Applicant respectfully requests the Commissioner to change the correspondence address for any and all patent applications and patents filed by STELLAR KINETICS LLC.

Applicant's new correspondence address is:

**Customer No. 35690**

B. Noël Kivlin

Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.

P.O. Box 398

Austin, Texas 78767-0398

(512) 853-8840

If there are any questions regarding this matter, please contact B. Noël Kivlin at the telephone number provided.

By: \_\_\_\_\_

Julia Coffalo

Title: \_\_\_\_\_

AUTHORIZED PERSON

Date: \_\_\_\_\_

16 JUN 2005

*Exhibit B***ASSIGNMENT OF PATENT RIGHTS**

For good and valuable consideration, the receipt of which is hereby acknowledged, Virtual Silicon Technology, Inc. having offices at 2215-B Renaissance Drive, Suite 5, Las Vegas, NV 89119, ("*Assignor*"), does hereby sell, assign, transfer and convey unto Stellar Kinetics LLC, a Nevada limited liability company, having an office at 2215-B Renaissance Drive, Suite 5, Las Vegas, NV 89119 ("*Assignee*") or its designees, all of Assignor's right, title and interest in and to the patent applications and patents listed below, any patents, registrations, or certificates of invention issuing on any patent applications listed below, the inventions disclosed in any of the foregoing, any and all counterpart United States, international and foreign patents, applications and certificates of invention based upon or covering any portion of the foregoing, and all reissues, re-examinations, divisionals, renewals, extensions, provisionals, continuations and continuations-in-part of any of the foregoing (collectively "*Patent Rights*");

| <u>Patent or Application No.</u> | <u>Country</u> | <u>Filing Date</u> | <u>Title and Inventor(s)</u>                                                                                                 |
|----------------------------------|----------------|--------------------|------------------------------------------------------------------------------------------------------------------------------|
| 60/154,155                       | US             | 9/15/1999          | Simple method for forming an EEPROM cell together with transistors for peripheral circuits; by John Caywood; Gregorio Spadea |
| 6,451,652                        | US             | 09/07/2000         | Method for forming an EEPROM cell together with transistor for peripheral circuits; by John Caywood; Gregorio Spadea         |
| 60/244,620                       | US             | 10/30/2000         | EEPROM and flash memory; by Albert Bergemont; Greg Spadea                                                                    |
| 6,606,265                        | US             | 10/30/2001         | Common source EEPROM and flash memory; by Albert Bergemont; Gregorio Spadea                                                  |
| PCT/US01/45319                   | WO             | 10/30/2001         | Common source EEPROM and flash memory; by Albert Bergemont; Gregorio Spadea                                                  |
| 01 993 004.9                     | EP             | 10/30/2001         |                                                                                                                              |

|                |    |            |                                                                                                                                                |
|----------------|----|------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 60/323,612     | US | 9/19/2001  | Non-volatile memory element;<br>by Glen Rosendale                                                                                              |
| 6,809,965      | US | 09/18/2002 | Control circuitry for a non-<br>volatile memory; by Glen Ar-<br>nold Rosendale                                                                 |
| PCT/US02/30043 | WO | 9/19/2002  | Control circuitry for a non-<br>volatile memory; by Glen A.<br>Rosendale                                                                       |
| NI-192309      | TW |            |                                                                                                                                                |
| 60/323,574     | US | 9/19/2001  | Methodology to optimize<br>CMOS ASIC library copper<br>power bus widths                                                                        |
| 6,687,880      | US | 09/16/2002 | Integrated circuit having a re-<br>duced spacing between a bus<br>and adjacent circuitry; by Bil-<br>lie Jean Rivera; William<br>Gordon Walker |
| PCT/US02/29572 | WO | 9/17/2002  | Integrated circuit having a re-<br>duced spacing between a bus<br>and adjacent circuitry; by Bil-<br>lie Jean Rivera; William<br>Gordon Walker |
| 60/373,744     | US | 4/17/2002  | Low power 5-volt input buffer;<br>by Mike McManus; Byungba<br>Joo                                                                              |
| 6,844,770      | US | 04/16/2003 | Circuitry to provide a low<br>power input buffer; by Michael<br>J. McManus                                                                     |
| PCT/US03/12142 | WO | 4/17/2003  | Circuitry to provide a low<br>power input buffer; by Michael<br>J. McManus                                                                     |

|                |    |            |                                                                                                                                                                       |
|----------------|----|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6,657,880      | US | 12/04/2002 | SRAM bit line architecture; by John M. Callahan                                                                                                                       |
| 60/291,457     | US | 5/15/2001  | High voltage N-channel LDMOS devices built in a deep submicron CMOS process; by Greg Spadea                                                                           |
| PCT/US02/15456 | WO | 5/14/2002  | High voltage N-channel LDMOS devices built in a deep submicron CMOS process; by Gregorio Spadea                                                                       |
| 10/147,329     | US | 5/15/2002  | High Voltage N-Channel LDMOS Devices Built in a Deep Submicron CMOS; by Gregorio Spadea                                                                               |
| 60/393,088     | US | 6/27/2002  | 3.3V 0.13um process high speed comparator of very wide common mode input differential signal; by Olivier Saint-Luc; Jackie Chu                                        |
| 10/609,006     | US | 6/26/2003  | Circuitry and method to provide a high speed comparator for an input stage of a low-voltage differential signal receiver circuit; by Olivier A. Saint-Luc; Jackie Chu |
| PCT/US03/20253 | WO | 6/27/2003  | Circuitry and method to provide a high speed comparator for an input stage of a low-voltage differential signal receiver circuit; by Olivier A. Saint-Luc; Jackie Chu |



|            |    |           |                      |
|------------|----|-----------|----------------------|
| 10/417,791 | US | 4/16/2003 | [title not provided] |
|------------|----|-----------|----------------------|

Except for US patent 6,451,652, which is co-owned by The John Millard and Pamela Ann Caywood 1989 Revocable Living Trust, Assignor represents, warrants and covenants that: (i) it is the sole owner, assignee and holder of record title to the Patent Rights identified above, (ii) it has obtained and properly recorded previously executed assignments for all patent applications and patents identified above as necessary to fully perfect its rights and title therein in accordance with governing law and regulations in each respective jurisdiction, and (iii) it has full power and authority to make the present assignment. Assignor shall indemnify and hold harmless Assignee for any breach of the foregoing.

Assignor further agrees to and hereby does sell, assign, transfer and convey unto Assignee all rights: (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past and future infringement of the Patent Rights, and (ii) to apply in any or all countries of the world for patents, certificates of invention or other governmental grants for the Patent Rights, including without limitation under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding. Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

Assignor will, at the reasonable request of Assignee and without demanding any further consideration therefor, do all things necessary, proper, or advisable, including without limitation the execution, acknowledgment and recordation of specific assignments, oaths, declarations and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights. Such assistance shall include providing, and obtaining from the respective inventors, prompt production of pertinent facts and documents, giving of testimony, execution of petitions, oaths, powers of attorney, specifications, declarations or other papers and other assistance reasonably necessary for filing patent applications, complying with any duty of disclosure, and conducting prosecution, reexamination, reissue, interference or other priority proceedings, opposition proceedings, cancellation proceedings, public use proceedings, infringement or other court actions and the like with respect to the Patent Rights.

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The terms and conditions of this Assignment shall inure to the benefit of Assignee, its successors, assigns and other legal representatives, and shall be binding upon Assignor, its successor, assigns and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at PALO ALTO, CA  
on March 30, 2005.

ASSIGNOR

By: 

Name: BARRY HOBERMAN

Title: PRESIDENT & CEO

(Signature MUST be notarized)

**CALIFORNIA ALL-PURPOSE ACKNOWLEDGMENT**

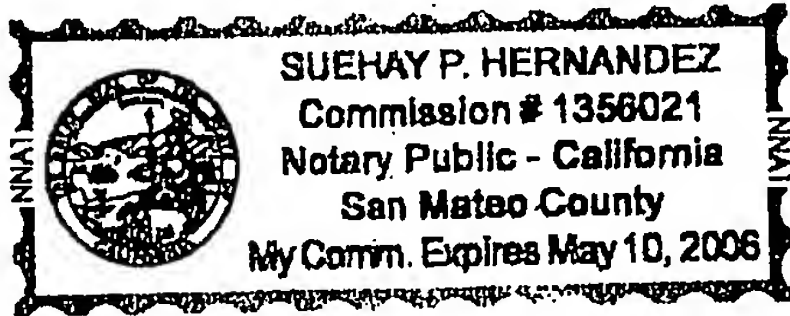
State of California

County of Santa Clara } ss.

On March 30, 2005 before me, Suehay P. Hernandez, Notary Public  
Date Name and Title of Officer (e.g., "Jane Doe, Notary Public")

personally appeared Barry Alan Haberberman  
Name(s) of Signer(s)

☐ personally known to me  
☒ proved to me on the basis of satisfactory evidence



to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

Suehay P. Hernandez  
Signature of Notary Public

**OPTIONAL**

*Though the information below is not required by law, it may prove valuable to persons relying on the document and could prevent fraudulent removal and reattachment of this form to another document.*

**Description of Attached Document**

Title or Type of Document: Assignment of Patent Rights

Document Date: 3-20-05 Number of Pages: 5

Signer(s) Other Than Named Above: Ø

**Capacity(ies) Claimed by Signer**

Signer's Name: \_\_\_\_\_

- ☐ Individual  
☐ Corporate Officer — Title(s): \_\_\_\_\_  
☐ Partner — ☐ Limited ☐ General  
☐ Attorney-in-Fact  
☐ Trustee  
☐ Guardian or Conservator  
☐ Other: \_\_\_\_\_

Signer Is Representing: \_\_\_\_\_

**RIGHT THUMBPRINT  
OF SIGNER**  
Top of thumb here